Amendments to the Specification

IN THE SPECIFICATION

Please replace the paragraph beginning on page 8, line 2 with the following amended paragraph:

In the arrangement of Fig. 9, a level of the power source voltage of the variable voltage power source 109 and an amplitude level (output level) of an output of the output full-bridge circuit 104 vary substantially in the same manner, so that the power consumption is not always kept at a level of the high volume as in the arrangement of Fig. 8. However, in the arrangement of Fig. 9, it is general that the variable voltage power source 109 is arranged as a servo circuit. Thus, a sufficient servo gain cannot be obtained in case of a low voltage, so that a voltage which has not been sufficiently servoed by the servo circuit is supplied to the switching amplification means. As a result, this raises the following deterioration of an audio performance: a distortion scale factor increases; S/N drops; and remaining noise increases. A data example of the distortion scale factor at this time is shown by a graph of Fig. ~~3~~ 5. As shown by ♦ of Fig. ~~3~~ 5, in a range where the output volume value is small, the distortion scale factor becomes larger as an output volume value becomes smaller.

Please replace the paragraph beginning on page 8, line 21 continuing to page 9, line 6 with the following amended paragraph:

Further, in the digital amplifier 201, when turning down the volume, the duty of the PWM signal inputted to the power source input terminal T00 is reduced as described above, so that a power level actually provided to a speaker, that is, a power level consumed in the output drive circuit ~~55~~ 205 becomes smaller. However, power

consumption in other circuits is the same as power consumption in the case where the volume is high. This is the same as in the case of Fig. 9. For example, the power consumption thereof is the same as the power consumption in the gate drive circuit 103 in the case of turning down the volume.

Please replace the paragraph beginning on page 9, line 7 with the following amended paragraph:

In view of the foregoing problems, the present invention was devised~~, and its main object is~~ to reduce the power consumption of a digital amplifier in case of turning down the volume. ~~A further object of~~ Further, the present invention ~~is to improve~~ improves an audio performance of the digital amplifier.

Please replace the paragraph beginning on page 20, line 17 continuing to page 21, line 6 with the following amended paragraph:

The foregoing arrangement is the same as the arrangement of the conventional digital amplifier ~~51~~ 201. However, in the digital amplifier 21 of the present invention, it is noteworthy that: a direct current power source voltage V1 that is supplied from a fixed-voltage power source (not shown) to the power source input terminal T1 is directly inputted to the lower gate drive circuit 29, and a voltage obtained by adding the power source voltage V1 to the power source voltage V0 is generated by the variable voltage power source 32 which functions as driving voltage variation means, and is inputted to the upper gate drive circuit 28. Thus, as in the variable voltage power source 30, the variable voltage power source 32 includes not only a low pass filter 33 constituted of a coil L24 and a capacitor C24 but also a capacitor C25 and a diode D.

Please replace the paragraph beginning on page 22, line 19 and continuing to page 23, line 10 with the following amended paragraph:

Thus, as shown in Fig. ~~5~~ 2, when the power source voltage V0 is high, a voltage by which the upper gate drive circuit 28 drives gates of the output transistors Q21 and Q23 is made higher, and when the power source voltage V0 is low, the voltage by which the upper gate drive circuit 28 drives the gates of the output transistors Q21 and Q23 is made lower. In this manner, it is possible to continuously keep the on-state gate voltage so high as to correspond to a predetermined voltage V1 which is constant. Thus, it is possible to minimize the voltage by which the upper gate drive circuit 28 drives the gates of the output transistors Q21 and Q23 without influencing the switching operation of the output transistors Q21 and Q23 when V1=2.5V, so that it is possible to reduce the power consumption of the upper gate drive circuit 28 in the case of turning down the volume (it is possible to reduce the power consumption so that its decrement corresponds to a voltage difference indicated by a shaded area in Fig. 5).

Please replace the paragraph beginning on page 43, line 11 with the following amended paragraph:

The variable voltage power source 30 demodulates the power source voltage V0 whose level is in proportion to the duty ratio of the PWM signal by causing a low pass filter 31 to smooth the PWM signal outputted from the PWM circuit ~~13~~ 13b. Further, the variable power source voltage 30 is connected to the variable voltage power source 32 as in the variable voltage power source 30 in the digital amplifier 21 of Example 1.